Abstract

The present invention discloses a multi-bit stacked-type non-volatile memory having a spacer-shaped floating gate and a manufacturing method thereof. The manufacturing method includes forming a patterned dielectric layer containing arsenic on a semiconductor substrate, wherein the patterned dielectric layer defines an opening as an active area. A dielectric spacer is formed on a side wall of the patterned dielectric layer and a gate dielectric layer is formed on the semiconductor substrate. A source/drain region is formed by thermal driving method making arsenic diffusion from the patterned dielectric layer into the semiconductor substrate. A spacer-shaped floating gate is formed on the side wall of the dielectric spacer and the gate dielectric layer. An interlayer dielectric layer is formed on the spacer-shaped floating gate. A control gate is formed on the interlayer dielectric layer and fills the opening of the active area.